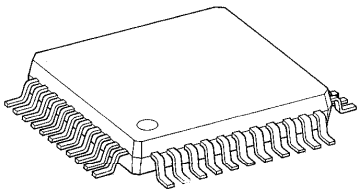
TENTATIVE TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC90A60U

DATA SLICE IC FOR VIDEO MULTIPLEX BROADCAST RECEIVER

TC90A60U is an IC for capturing Japan teletext and data broadcast (also EIA-516) signals superposed on video signals. Its main functions include sync separation, equalization, data and sampling clock generation, and error correction.
When connected in parallel to a microcontroller, the IC allows data capturing with a relatively small part count.



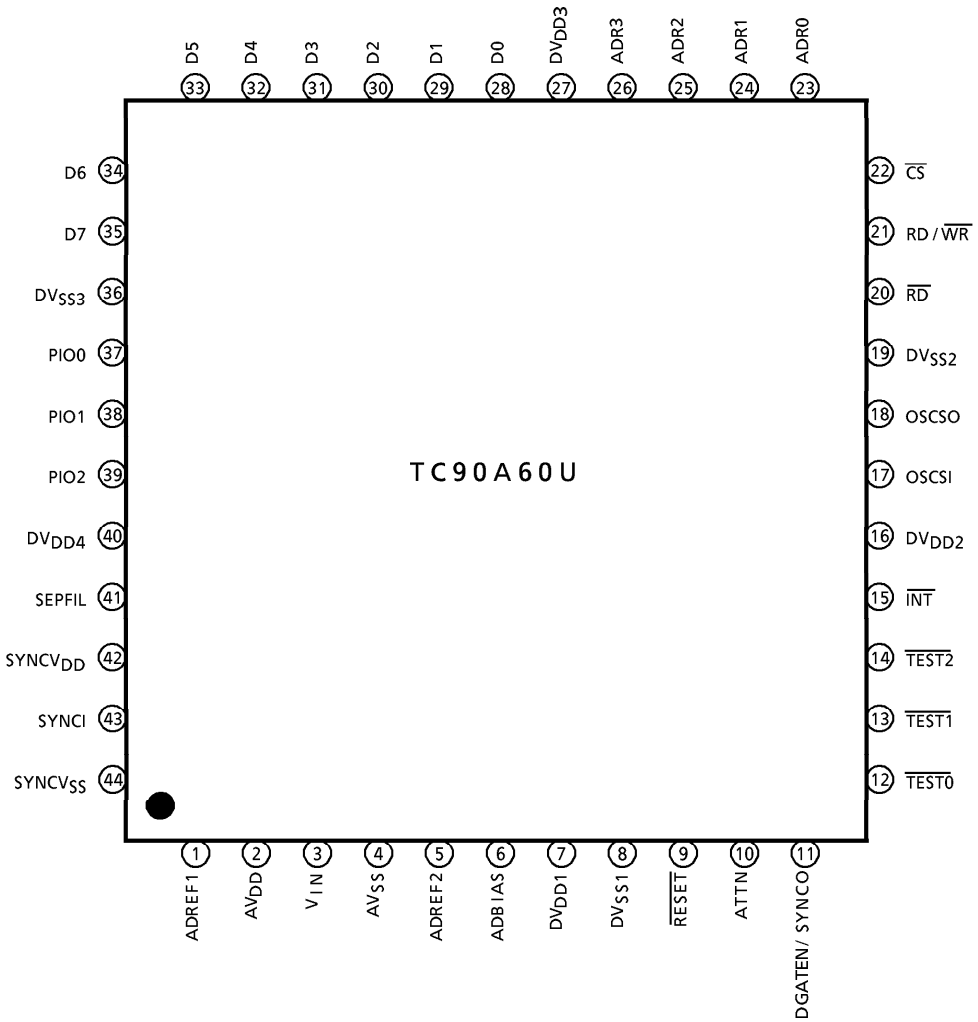
QFP44-P-1010-0.80

Weight : 0.5 g (Typ.)

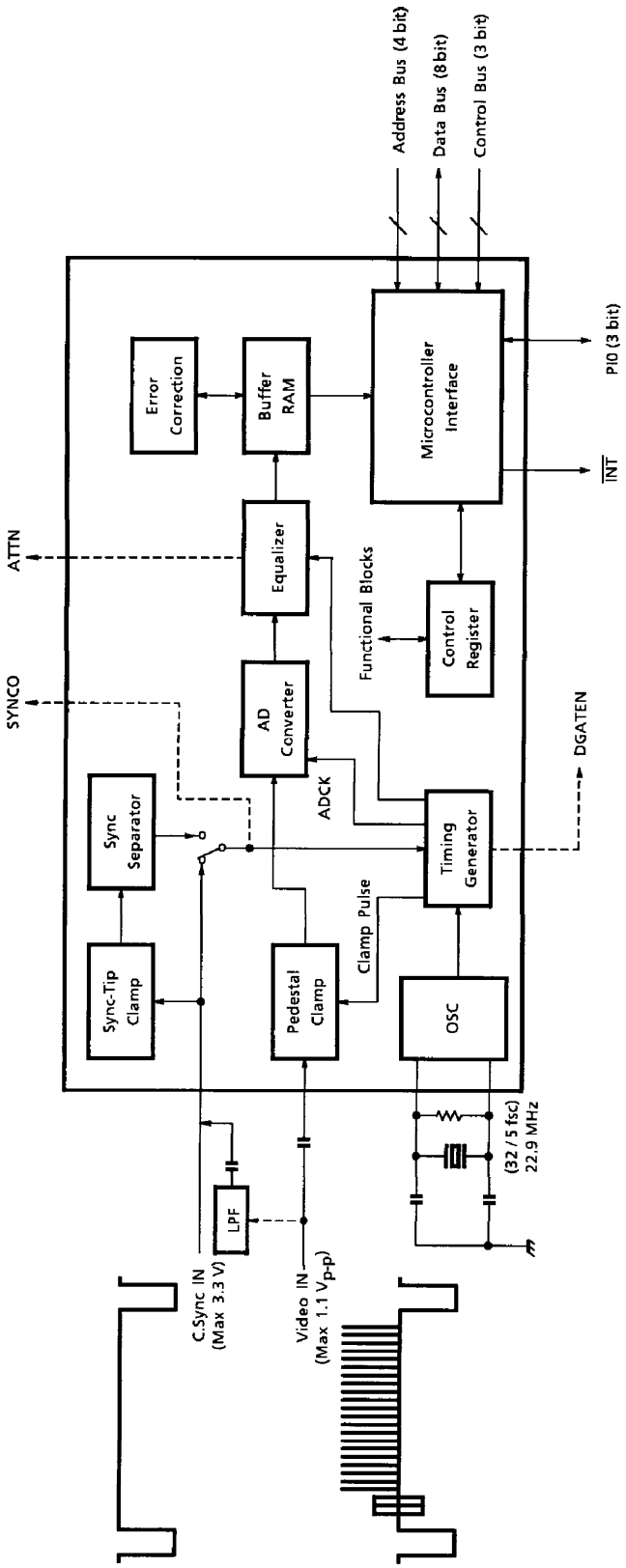
FEATURES

- Digital regeneration of Japan eletext and data broadcast (also EIA-516) data using a built-in AD converter
- Equalization using a 13-tap transversal filter (equalization range : $-0.5 \sim 1.5\ \mu s$)
- Buffer memory which accommodate 8 data packets
- Error correction circuit
- Framing code detection
- Sync separator circuit
- Parallel interface (8 bits for data, 4 bits for address and 3 bits for control)
- 3.3 V single power supply

PIN ASSIGNMENT



BLOCK DIAGRAM



TC90A60U—3

OVERVIEW OF TC90A60U INTERNAL BLOCKS

1. AD Converter

   TC90A60U incorporates a 6-bit serial high-speed AD converter, which converts composite video signals superposed with Japan teletext signals.
   (Sampling frequency : 16 / 5 fsc = 11.454545 MHz)

2. System Clock Oscillator

   A crystal oscillator is used to generate clocks such as sampling clock for the AD Converter.
   (Oscillation frequency : 32 / 5 fsc = 22.909088 MHz)

3. Data regeneration and equalization

   Video multiplex signals are sampled and converted in the AD converter.
   The data is equalized using the built-in 13-tap transversal filter so as to recognize 0 or 1 correctly.
   The equalization range is $-0.5 \sim +1.5\ \mu s$.

4. Data capture

   Equalized multiplex data on lines 10 H~16 H and 21 H (any lines within 10 H~25 H can be selected using the Control Register) are captured into the buffer memory which accommodates 8 data packets.
   A single packet consists of 35 bytes.

5. Sync Separator

   The sync separator separates composite sync signals from the luminance signals which are removed of color signal in the LPF external to the IC.

6. Microcontroller Interface

   TC90A60U incorporates a parallel interface to allow connection to a microcontroller.

7. Monitors and control pins

   TC90A60U incorporates pins for monitoring internal operation and controlling external components.

   ATTN : Outputs video attenuator control signals.
   Also used for monitoring system clock (22.9 MHz).

   DGATEN / SYNCO : Used for monitoring sync separation circuit output signals or data capture timing.

   PIO [2~0] : Used as general-purpose input / output pins.

   For details of each block, please refer to functional description.

- **PIN DESCRIPTION**

	PIN No.	PIN NAME	I/O	FUNCTION	INPUT	OUTPUT
ADC	1	ADREF1		ADC reference pin (Connected to GND via a capacitor)		
	2	AV_{DD}		Analog V_{DD} pin for ADC	1.1 V_{p-p}	
	3	V_{IN}	I	Analog input pin for ADC (Dynamic input range : 1.1 V_{p-p})		
	4	AV_{SS}		Analog GND pin for ADC		
	5	ADREF2		ADC reference pin (Connected to GND via a capacitor)		
	6	ADBIAS		ADC bias pin (Connected to GND via a capacitor)		
Testing	9	RESET	I	System reset pin (Active Low)	5 V withstand voltage	
	10	ATTN	O	Video attenuator output pin (Active LOW)		V_{DD}
	11	DGATEN / SYNCO	O	Teletext signals removing gate signal output pin (default setting)		V_{DD}
			O	Sync separation signal output pin		V_{DD}
	12	TEST0	I	Test input pin 0 (Fix to HIGH in normal operation)		
	13	TEST1	I	Test input pin 1 (Fix to HIGH in normal operation)		
	14	TEST2	I	Test input pin 2 (Fix to HIGH in normal operation)		
Oscillation	16	DV_{DD2}		Digital V_{DD}		
	17	OSCSI	I	System clock oscillation circuit input		
	18	OSCSO	O	System clock oscillation circuit input (32 / 5 fsc)		
	19	DV_{SS2}		Digital GND		

	PIN No.	PIN NAME	I/O	FUNCTION	INPUT	OUTPUT
Microcontroller Interface and Logic	7	DV_{DD1}		Digital V_{DD}		
	8	DV_{SS1}		Digital GND		
	15	INT	O	Interrupt signal output pin (open-drain buffer)		5 V withstand voltage
	20	RD	I	Read enable signal input pin (Active Low)	5 V withstand voltage	
	21	RD / WR	I	Write enable signal input pin (Active Low)	5 V withstand voltage	
	22	CS	I	Chip select input pin (Active Low)	5 V withstand voltage	
	23	ADR0	I	Address Bus 0 control	5 V withstand voltage	
	24	ADR1	I	Address Bus 1 control	5 V withstand voltage	
	25	ADR2	I	Address Bus 2 contro	5 V withstand voltage	
	26	ADR3	I	Address Bus 3 control	5 V withstand voltage	
	27	DV_{DD3}		Digital V_{DD}		
	28	D0	I/O	Data Bus 0	5 V withstand voltage	V_{DD}
	29	D1	I/O	Data Bus 1	5 V withstand voltage	V_{DD}
	30	D2	I/O	Data Bus 2	5 V withstand voltage	V_{DD}
	31	D3	I/O	Data Bus 3	5 V withstand voltage	V_{DD}
	32	D4	I/O	Data Bus 4	5 V withstand voltage	V_{DD}
	33	D5	I/O	Data Bus 5	5 V withstand voltage	V_{DD}
	34	D6	I/O	Data Bus 6	5 V withstand voltage	V_{DD}
	35	D7	I/O	Data Bus 7	5 V withstand voltage	V_{DD}
	36	DV_{SS3}		Digital GND		
	37	PIO0	I/O	General-purpose input / output pin 0 (input pin by default)	5 V withstand voltage	V_{DD}
	38	PIO1	I/O	General-purpose input / output pin 1 (input pin by default)	5 V withstand voltage	V_{DD}
	39	PIO2	I/O	General-purpose input / output pin 2 (input pin by default)	5 V withstand voltage	V_{DD}
	40	DV_{DD4}		Digital V_{DD}		
Sync Separation	41	SEPFIL		Sync separation filter pin (Connected to GND via a capacitor)		
	42	$SYNCV_{DD}$		Analog V_{DD} for sync separator		
				Composite sync signal (C.Sync) input pin (default setting)	3.3 V withstand voltage	
	43	SYNCI	I	Sync separation luminance signal input pin	1 V_{p-p}	
	44	$SYNCV_{SS}$		Analog GND for sync separation		

MAXIMUM RATINGS (Ta = 25°C)

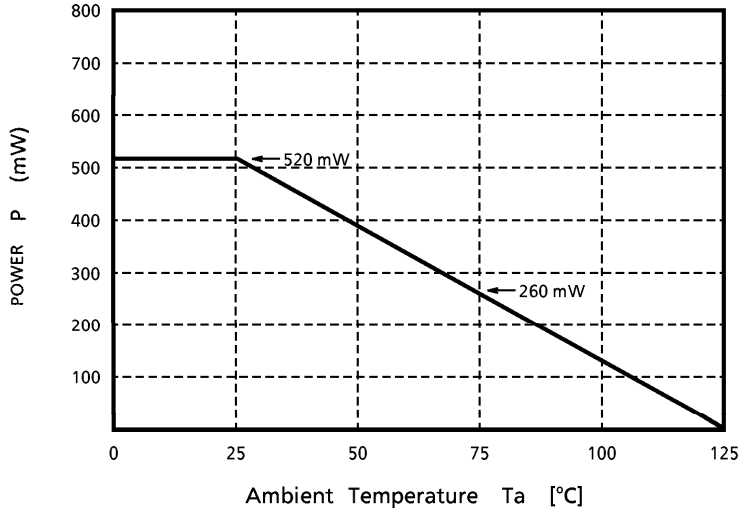
PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{DD}	V_{SS}~V_{SS} + 4.5	V
Input Voltage	V_{IN1}	− 0.3~V_{DD} + 0.3	V
	V_{IN2}	− 0.3~5.5 (Note 1)	V
Power Dissipation	P_D	520 (Note 2)	mW
Storage Temperature	T_{stg}	− 55~125	°C

(Note 1) : Applicable to ADR [3~0], D [7~0] CS, RD, RD / WR, PIO [2~0] RESET
(Note 2) : When the device is used in an ambient temperature of 25 °C or higher, the rated value should be calculated by decrementing 5.20 mW per 1 °C.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT
Power Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Input Voltage	V_{IN}	0	—	V_{DD}	V
Operating Temperature	V_{opr}	− 20	—	75	°C

Package thermal resistance characteristics : QFP44-P-1010-0.80



- **PRECAUTIONS**

■ Do not apply voltage to any pin or pins while the power supply to the IC is off.

■ D [7~0], PIO [2~0] should not be pulled up to 5 V. These pins are used both for input and output : their input withstand voltage is 5 V and their HIGH output voltage is V_{DD} (3.3 V). Pulling these pins up to 5 V results in unstable operation.

Pulling-up I/O pins with 5-V withstand voltage

PIN	PULL-UP		RECOMMENDED RESISTANCE
	3.3 V	5 V	
ADR [3~0]	○	○	3.3 kΩ or higher
CS	○	○	3.3 kΩ or higher
RD	○	○	3.3 kΩ or higher
RD / WR	○	○	3.3 kΩ or higher
RESET	○	○	3.3 kΩ or higher
D [7~0]	○	×	3.3 kΩ or higher
PIO [2~0]	○	×	3.3 kΩ or higher

- I/O REGISTERS

1. Write Registers

Consecutive Writes

PIN STATE RD/WR	ADR	SYM-BOL	FUNCTION	SW NAME	B7	B6	B5	B4	B3	B2	B1	B0	REMARKS	INITIAL VALUE
WR	0Hex	W00	Selects capture line.	ZDIP	0	0	0	0	0	0	0	0	Bits B7~B0 corresponds to line buffers 7~0, respectively. 1 : Captures 0 : Does not capture.	00Hex
WR	0Hex	W01	Selects C.Sync input mode.	SYNCSEP								0	0 : C.Sync Input Mode 1 : Internal Sync Separation Mode	0
			Selects C.Sync input signal polarity.	SYNCPOL							0		0 : Negative 1 : Positive	0
			Selects DGATEN (Pin 11) output signal.	DGATENSW						0			0 : DGATEN (capture timing monitor) 1 : SYNCO (sync signal monitor)	0
			Selects sync separation level.	SEPLEV					0				Selects slice level for the internal sync separation circuit. (Refer to 1.7.)	0
			Selects error correction mode.	BESTC				0					0 : Carries out BEST correction. 1 : Does not carry out BEST correction.	0
			Selects INT signal deassertion mode.	INTSW		0							1 : Automatically deasserts INT signal approximately 260 ns after its occurrence.	0
			Selects ATTN (Pin 10) output signal.	ATTNSW	0								0 : ATTN 1: System clock monitor	0
							0						This bit must be fixed to 0.	
WR	0Hex	W02	Selects framing code protection mode.	FC1STN								0	0 : Only the framing code detected first is valid. 1 : All framing codes are valid.	0
			Selects framing code regeneration mode.	FCH0GO							0		0 : Framing code real-time generation mode 1 : Framing code consecutive regeneration mode	0
			Selects fixed / variable capture line.	VARLN				0					0 : 10H~16H and 21H (fixed) 1 : Variable	0
					0	0	0		0	0			These bits must be fixed to 0.	0
WR	0Hex	W03	Selects Line 0 / Line 1 capture.	LINE01	Line 1				Line 0				Selects the line to be captured into the buffer using the corresponding four bits. ZDIP is used to select whether or not to capture the selected line. The line to be captured can be obtained by adding an offset of 10 to the 4-bit value. (e.g. If 0101Bin is specified, 5H + 10H, that is, 15H, is selected.) The same line cannot be selected to be captured into multiple buffers.	10Hex
WR	0Hex	W04	Selects Line 2 / Line 3 capture.	LINE23	Line 3				Line 2					32Hex
WR	0Hex	W05	Selects Line 4 / Line 5 capture.	LINE45	Line 5				Line 4					54Hex
WR	0Hex	W06	Selects Line 6 / Line 7 capture.	LINE67	Line 7				Line 6					B6Hex
WR	0Hex	W07	Selects framing code.	FCCODE	1	1	1	0	0	1	0	1	Selects framing code.	E5Hex

WR	1Hex	W10	Selects line buffer to be read out.	INPH	0	0	0	0	0	0	0	0	Selects line buffer (7~0) to be read out on R30 using the lower three bits.	00Hex
WR	1Hex	W11	Selects byte address.	ARSTA	0	0	0	0	0	0	0	0	Selects the byte address of the line buffer to start access (00Hex~22Hex) using the lower six bits. 00Hex~22Hex	00Hex

WR	2Hex	W20	Resets flags.	FLGRST						0			1 : Resets Capture Completion Flag and Error Correction Completion Flag.		0
			Deasserts INT signal.	INTRST					0				1 : Deasserts INT signal.		0
			Sets HLDA internally.	HLDASET				0					1 : HLDA signal is set internally in the IC. (Refer to 2.2.)		0
			Resets HLDA internally.	HLDARST			0						1 : HLDA signal is reset internally in the IC. (Refer to 2.2.)	Do not simultaneously set these two bits to 1.	0
			Sets COR internally.	CORSET		0							1 : COR signal is set internally in the IC. (Refer to 2.2.)		0
					0				0			0	These bits must be fixed to 0.		0

WR	3Hex	W30	Internal RAM Write access	ARRDW									Writes data to the internal line buffer specified in W10 and W11.	

(Note) : Registers W00~W07, W10~W11, W40~W41, R10~R11 and R20~R2F respectively, which share the same address, are written to or read from consecutively. If an access to a different address occurs during the consecutive Read / Write access, the Read / Write resumes by accessing the first register.

1. Write Registers (continued)

Consecutive Writes

PIN STATE RD/WR	ADR	SYM-BOL	FUNCTION	SW NAME	B7	B6	B5	B4	B3	B2	B1	B0		INITIAL VALUE
WR	4Hex	W40	General-purpose port output data setting	POD0								0	Pin 37 PIO0 output 0 : LOW 1 : HIGH	0
				POD1							0		Pin 38 PIO1 output 0 : LOW 1 : HIGH	0
				POD2						0			Pin 39 PIO2 output 0 : LOW 1 : HIGH	0
					0	0	0	0	0				These unused bits must be fixed to 0.	0
WR	4Hex	W41	General-purpose port mode setting	POCNT0								0	Pin 37 PIO0 Pin Mode 0 0 : Input port 1 : Output port	0
				POCNT1							0		Pin 38 PIO1 Pin Mode 0 0 : Input port 1 : Output port	0
				POCNT2						0			Pin 39 PIO2 Pin Mode 0 0 : Input port 1 : Output port	0
					0	0	0	0	0				These unused bits must be fixed to 0.	0
WR	5Hex	W50	Equalizer control	FAST					1				Equalization mode 0 : Low speed1 : High speed	1
				TGHN			1						0 : Fixed tap gain	1
				TRGSTN		1							0 : Equalizer stopped.	1
				RESETON	1								0 : Equalizer reset.	1
								1		1	1	1	These bits must be fixed to 1.	1
WR	6Hex	W60	Test register		1	1	1	1	1	1	1	1	All the bits must be fixed to 1.	FFHex
WR	6Hex	W61	Test register		0	0	0	0	0	0	0	0	All the bits must be fixed to 0.	00Hex
WR	7Hex	W70	Test register										Test register	
WR	7Hex	W71	Test register										When all the test pins (Pin 12~Pin 14) are pulled HIGH	
WR	7Hex	W72	Test register										(i.e. the device is in normal operation),	
WR	7Hex	W73	Test register										Inputting any value on W70~W73 has no effect.	

(Note) : Registers W00~W07, W10~W11, W40~W41, R10~R11 and R20~R2F respectively, which share the same address, are written to or read from consecutively. If an access to a different address occurs during the consecutive Read/Write access, the Read/Write resumes by accessing the first register.

2. Read Registers

PIN STATE RD/WR	ADR	SYM-BOL	FUNCTION	SW NAME	B7	B6	B5	B4	B3	B2	B1	B0	REMARKS
RD	8Hex	R00	Capture Completion Flag	TFLG									1 : Capture complete
			BEST Correction Completion Flag	CFLG									1 : BEST correction complete
			HLDA signal monitor	HLDA									1 : Line buffer internal access. (Refer to 2.2.)
			COR signal monitor	COR									1 : Correction is in progress. (Refer to 2.2.)
					×	×	×	×					Bits B7~B4 are undefined.
RD	9Hex	R10	Framing code detection result	FCDET									Stores framing detection result 0 : Normal 1 : Error Bits B7~B0 corresponds to line buffer 7~0, respectively.
RD	9Hex	R11	BEST correction result	BESTFLG									Stores BEST correction result 0 : Normal 1 : Error Bits B7~B0 corresponds to line buffers 7~0, respectively.
RD	AHex	R20	SI data and CI data	SI0	SI				Check				Outputs the first two bytes of the line buffer content before error correction.
RD	AHex	R21	(All line buffers)	CI0	CI				TF	IF	×	×	The bit sequence is inverted. (B7 becomes LSB.)
:		:		:	:				:				
RD	AHex	R2E		SI7	SI				Check				
RD	AHex	R2F		CI7	CI				TF	IF	×	×	
RD	BHex	R30	Receive data (line buffer data)	ARRDR	(MSB)							(LSB)	Outputs the content of the line buffer specified in W10 and W11. W11 (byte address) is automatically incremented on each consecutive access.
RD	CHex	R40	General-purpose port input data	PID0									1 : HIGH, 0 : LOW (Undefined when the port is used for output.)
				PID1									1 : HIGH, 0 : LOW (Undefined when the port is used for output.)
				PID2									1 : HIGH, 0 : LOW (Undefined when the port is used for output.)
					×	×	×	×	×				Bits B7~B3 are undefined.
RD	FHex	R70	Test Register		(MSB)							(LSB)	Outputs the content of W70.

Consecutive Writes

(Note) : Registers W00~W07, W10~W11, W40~W41, R10~R11 and R20~R2F respectively, which share the same address, are written to or read from consecutively. If an access to a different address occurs during the consecutive Read / Write access, the Read / Write resumes by accessing the first register.

FUNCTIONAL DESCRIPTION

1. Basic Functions

1.1 AD Converter Specifications (video input)

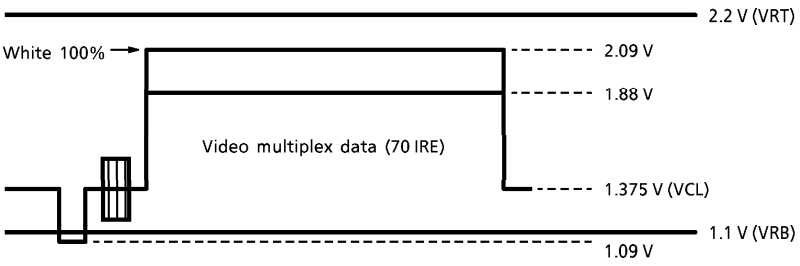
Data conversion range : 1.1 V ± 0.01 V (VRB) ~ 2.2 V ± 0.01 V (VRT)

Pedestal Clamp : 1.375 V ± 0.01 V (1 / 4 of data conversion range)

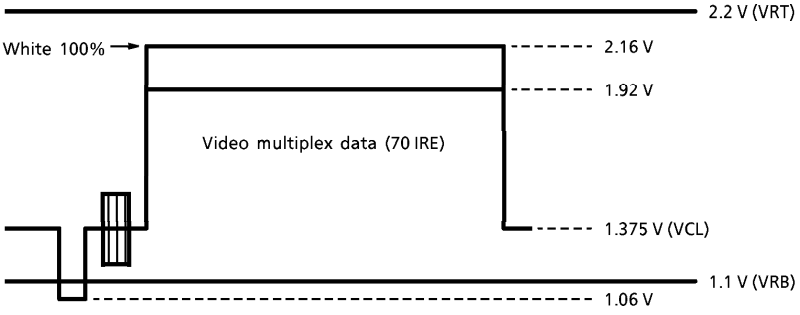
Data conversion rate : 16 / 5 fsc (11.454545 MHz)

- The difference between AD bottom range (VRB) and clamp level (VCL) is 0.25 V (35 IRE).
- The amplitude of video multiplex data is 70 IRE.

■ 1 V_{p-p} Video Input



■ 1.1 Vp-p Video Input



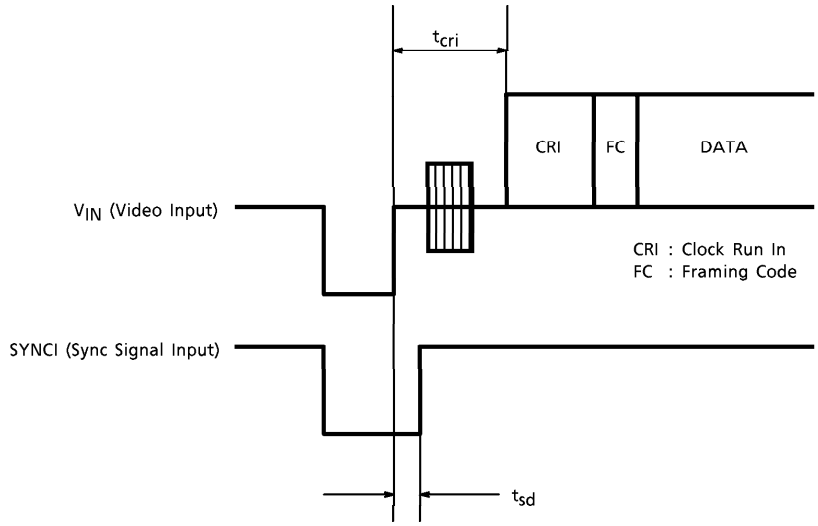
1.2 System Clock Oscillator

TC90A60U uses a crystal resonator to generate 32 / 5 fsc source clock (4 times teletext data rate 8 / 5 fsc).
The crystal resonator to be used should observe the following specifications.

Crystal resonator specifications

PARAMETER	SPECIFICATION
Nominal Frequency (f_0)	22.909088 MHz
Load Capacitance	30.0 pF ± 0.5 pF
Frequency Deviation	± 20 ppm
Equivalent Resistance	30 Ω or below, serial
Temperature Characteristics	± 30 ppm, – 20 °C~75 °C (reference : 25 °C)

1.3 Video Input and Sync Input



PARAMETER	SYMBOL	MIN	TYP.	MAX	UNIT
CRI position	t_{cri}	27	29	32	TC (*)
SYNC delay	t_{sd}	—	—	0.8	μs

(*) : TC = 1 / 364 f_H μs

1.4 Equalization Circuit

The equalization circuit incorporates a 13-tap transversal filter. The equalization range is −0.5 μs~ +1.5 μs. Equalization takes approximately 0.1 s~2 s to complete. (Equalization is almost complete when 32 to 128 lines are captured.)
The filter modulus cannot be changed by the user.
If the tap gain of the filter is too high, ATTN (Pin 10) is pulled LOW.
By attaching an attenuator circuit external to the IC, the LOW signal can be used to control the input amplitude and thereby to prevent overflows.

1.5 Error Correction Circuit

Error correction is performed on each data packet (272,190) using shortened cyclic code for difference set.
The data after error correction is written in the 8 built-in line buffers.
Error correction takes approximately 100 μs for each line buffer.

1.6 Line Buffers

TC90A60U incorporates 8 line buffers, each of which consists of 35 bytes.
Each line buffer corresponds to a single data line : which line buffer corresponds to which data line can be set in software. A single data line cannot be set to be captured into multiple line buffers. Thus it is not allowed, for instance, to capture 10H into all the 8 line buffers.
TC90A60U is not capable of accumulating more than 1-field data. A set of data usually extends continuously across many fields. Thus capturing such a set of data requires field-by-field access to TC90A60U and storing the captured data in a larger external memory.

- Line buffer data configuration

  The two tables below show the contents to be captured into a line buffer before error correction (left) and the contents of the line buffer after error correction (right) in ordinary teletext broadcast.

Line buffer content before error correction

BYTE ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0
00hex	b0	b1	b2	b3	b4	b5	b6	b7
	SI				Check			
01hex	b0	b1	b2	b3			b0	b1
	CI				TF	IF	DB1	
02hex	b2	b3	b4	b5	b6	b7	b0	b1
	DB1						DB2	
≀	≀							
17hex	b2	b3	b4	b5	b6	b7	0	1
	DB22						CB	
18hex	2	3	4	5	6	7	8	9
	CB : Check bit (82 bit)							
≀	≀							
21hex	74	75	76	77	78	79	80	81
	CB : Check bit (82 bit)							
22hex								b0
	Unused (*2)							(*1)

Line buffer content after error correction

BYTE ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0
00hex	b5	b4	b3	b2	b1	b0		
	Check		SI				Unused	
01hex			b3	b2	b1	b0	b7	b6
	IF	TF	CI				Check	
02hex	b7	b6	b5	b4	b3	b2	b1	b0
	DB1							
≀	≀							
17hex	b7	b6	b5	b4	b3	b2	b1	b0
	DB22							
18hex								
	Unused							
≀	≀							
21hex								
	Unused							
22hex								
	Unused							

(*1) : Stores Framing Code Information (FCI). (See next page for details.)
(*2) : Values of unused bits are undefined.

- Data line and line buffer address

  Which data line will be captured into which line buffer can be set as shown in the below table.

ADDRESS	DATA LINE	
DECIMAL	VARLN = 0	VARLN = 1
0	10H	Set using LINE01 [3~0].
1	11H	Set using LINE01 [7~4].
2	12H	Set using LINE23 [3~0].
3	13H	Set using LINE23 [7~4].
4	14H	Set using LINE45 [3~0].
5	15H	Set using LINE45 [7~4].
6	16H	Set using LINE67 [3~0].
7	21H	Set using LINE67 [7~4].

■ Control registers

VARLN : VARLN (0Hex W02 B4) : Selects 0: fixed line capture / 1 : variable line capture.

LINE01~67 : LINE01~LINE67 : (0Hex W03~W06) : Selects the line to be captured. The line to be captured is obtained by adding an offset of 10 to the specified 4-bit value. A single data line cannot be set to be captured into multiple line buffers.
(If this is attempted, a capture error is assumed to have occurred and the buffer content will be undefined.)

- Framing Code Information (FCI)

  Framing code information is captured into line buffer (22Hex B0) before performing error correction. The FCI value has the following meanings :

0 : FCI not detected.

FCI is not properly captured or the data line does not contain teletext data.

1 : FCI detected.

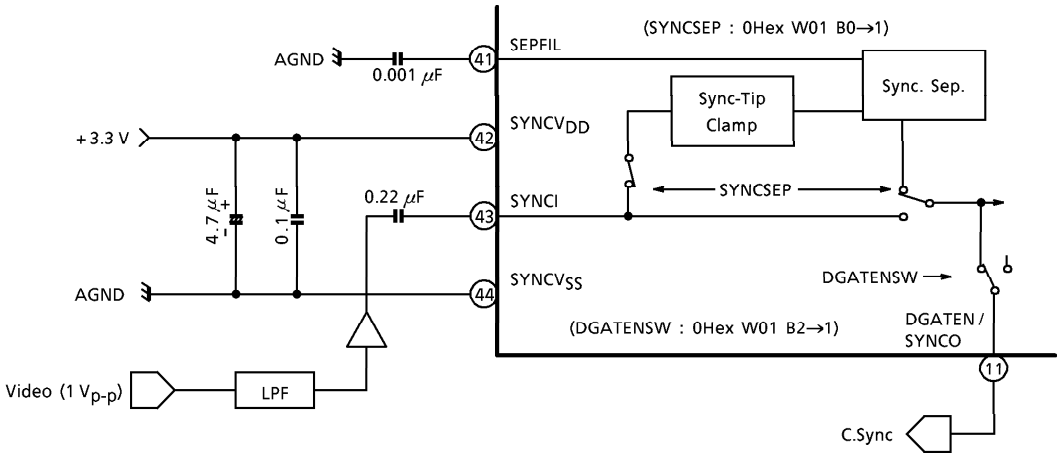
(Note) : Error correction is not performed on line buffers for which FCI = 0 (i.e. an error is detected).

■ FCI for Line Buffers 7~0 are stored in FCDET (9Hex R10) with their polarity inverted. FCDET[B7~B0] corresponds to Line Buffers 7~0, respectively.

1.7 Sync Separation Circuit

TC90A60U incorporates a sync separation circuit to extract composite sync signals from luminance signals. It also incorporates a Sync-Tip Clamp to allow video input signals to be sliced at a fixed voltage and thereby sync signals to be generated. The slice level is automatically switched between two modes according to the Sync amplitude.

Block diagram of sync separation circuit and its peripherals



■ Design specification

(The values are given for reference and does not necessarily represent the IC's actual performance.)

Input signal

Input amplitude : Luminance signal (140 IRE) 0.8 V_{p-p}~2 V_{p-p} (1 V_{p-p} is recommended.)

Composite video signals should be input to the IC via a buffer (Zo = 300 Ω or below recommended) after removing color signal in the LPF.

Clamp voltage : Sync. Tip = 1.089 V (V_{DD} = 3.3 V)

Slice level (when V_{DD} = 3.3 V)

(1) Sync. amplitude : 229 mV_{P-P} or above

H_f (leading edge detection) : Sync-Tip + 129 mV

H_f (trailing edge detection) : Sync-Tip + 157 mV

Hysteresis : 28 mV

(2) Sync. amplitude : 200 mV_{P-P} or below (0Hex W01 B3 SEPLEV = 0)

L_f : Sync-Tip + 57 mV

L_r : Sync-Tip + 71 mV

Hysteresis : 14 mV

(2)' Sync. amplitude : 200 mV_{P-P} or below (0Hex W01 B3 SEPLEV = 1)

L_f : Sync-Tip + 86 mV

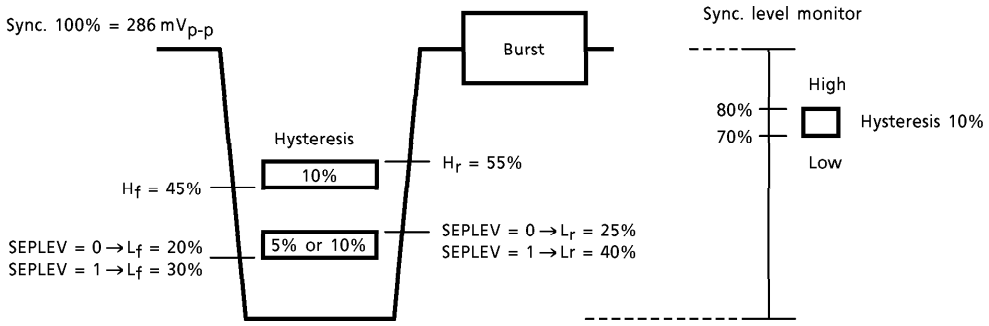
L_r : Sync-Tip + 114 mV

Hysteresis : 28 mV

(*) : Either (2) or (2)' can be selected using the control register.

The slice level can be expressed in percentage as shown below (when input signal is NTSC 1 V_{P-P}).

NTSC 1 V_{P-P} input



Sync signal output

- Signal output delay : Within slice level + 100 ns
- Signal jitter : Within 10 ns

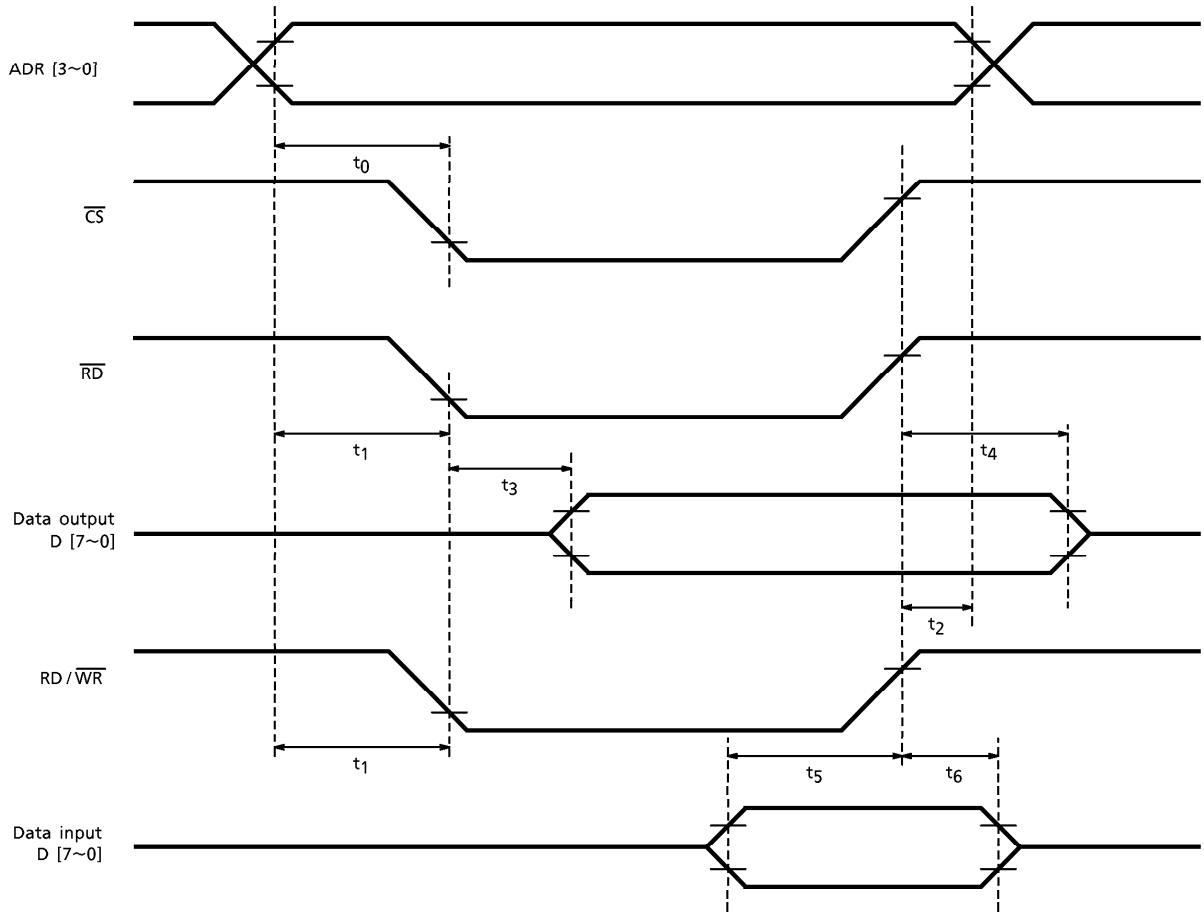
■ Precautions regarding the sync separation circuit

- The values given in the design specification are for reference and do not necessarily represent the IC's actual performance.
- Sync signal is not output when there is no input signal.
- It takes several hundred ms (depending on the external coupling capacitance) for the clamp voltage to be stable, during which time valid output signal is not available.
- When the input signal is switched to that of a different amplitude, Sync. level may not be monitored correctly during the first field input.

1.8 Microcontroller Interface

TC90A60U incorporates 4-bit address bus, 8-bit data bus, 3-bit control bus and 1-bit interrupt output bus so as to allow parallel interfacing to a microcontroller.

■ Timing chart



Microcontroller Interface AC Characteristics (Design Specification)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Address Setup Time Prior to CS	t_0	0	—	ns
Address Setup Time Prior to RD / WR	t_1	0	—	ns
Address Hold Time After Deactivation of RD / WR / CS	t_2	0	—	ns
Data Setup Time After RD	t_3	—	40	ns
Data Hold Time After Deactivation of RD / CS	t_4	3	18	ns
Data Setup Time Prior to Deactivation of WR	t_5	20	—	ns
Data Hold Time After Deactivation of WR	t_6	0	—	ns

- Interface Access Procedure

  ① Parallel ports are used for accessing I/O registers within the IC.

  ② CS is asserted when accessing the IC.

  ③ The IC acknowledges the register to be accessed by the conditions of ADR, RD and RD/WR.

  ④ When RD is asserted along with CS, the IC acknowledges the access as a Read access and outputs the contents of the registers specified using ADR and RD on the data bus.

  ⑤ When either RD or CS is deasserted, the IC acknowledges the Read access to be completed and deactivates output on the data bus.

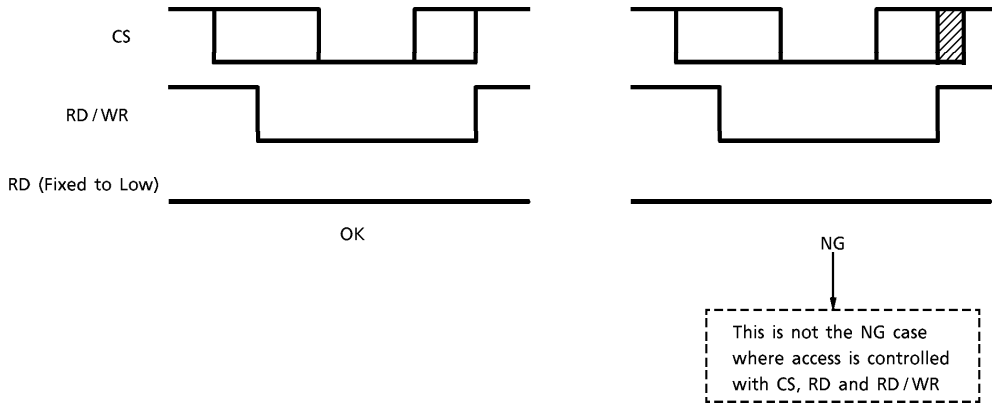
  ⑥ When RD/WR is asserted along with CS, the IC acknowledges the access as a Write access and get ready to write data in the registers specified using ADR and RD/WR.

  ⑦ The data is latched into the registers on deassertion of RD/WR.

- Controlling Read/Write Access using CS and RD/WR only

  Read/Write access to TC90A60U, which is usually controlled using CS, RD and RD/WR, can also be controlled with CS and RD/WR only. In that case, RD Pin must be grounded to GND, High on RD/WR Pin indicates a Read access and Low on the same pin indicates a Write access, and t3 and t4 on the preceding page depend not assertion/deassertion timing of CS, not on RD.

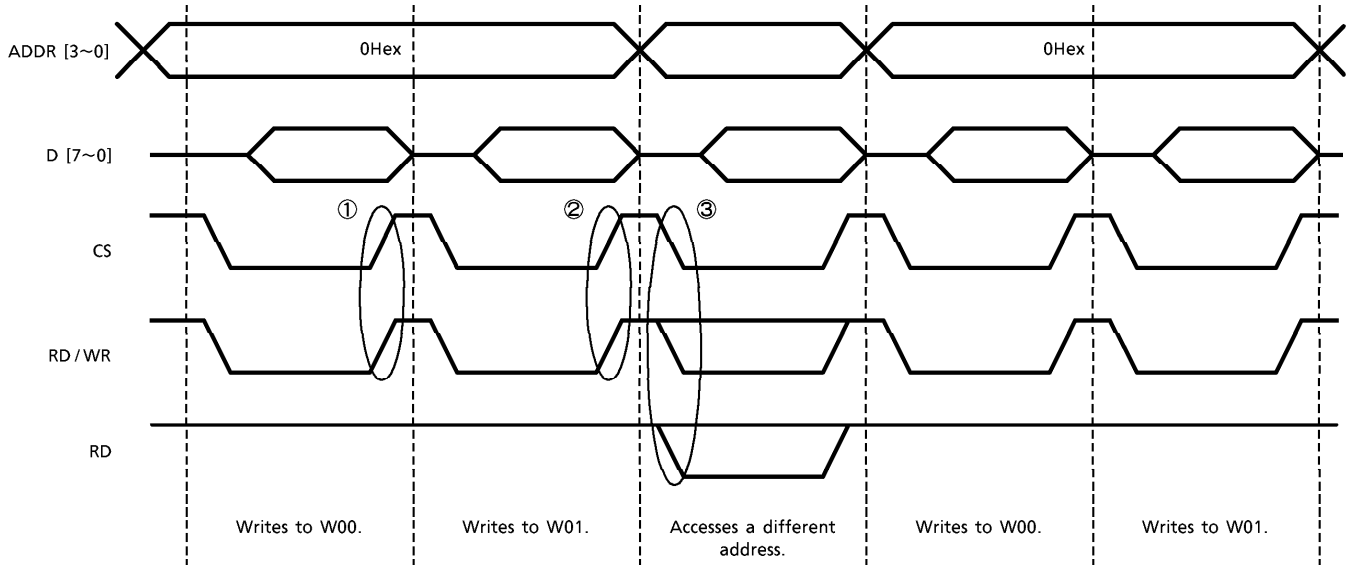
  When access is controlled with CS and RD/WR only, an access is invalid if RD/WR is deasserted before CS is deasserted. This is not the case where access is controlled with CS, RD and RD/WR.



- Consecutive Read / Write from / to the Same Address

  Registers W00~W07, W10~W11, W60~W61, W70~W73, R10~R11, R20~R2F and R40~R41 respectively share the same address and thus the address needs to be accessed consecutively. If an access to a different address occurs during the consecutive Read / Write access, the Read / Write resumes by accessing the first register.

- Example : An access to a different address occurs while accessing 0Hex registers.



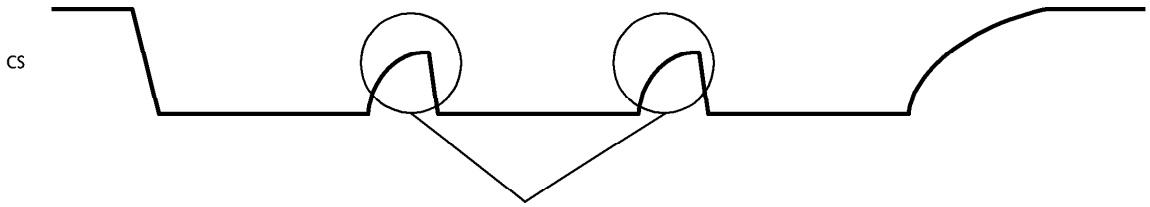
① When a Write to W00 is complete, the address of the register to be accessed next is counted up to W01. The address is counted up in synchronization with the rising edges of CS.

② When a Write to W01 is complete, the address of the register to be accessed next is counted up to W02.

③ If an access to a different address occurs during a consecutive Read / Write access, the Read / Write resumes by accessing the first register (W00 in the above example).

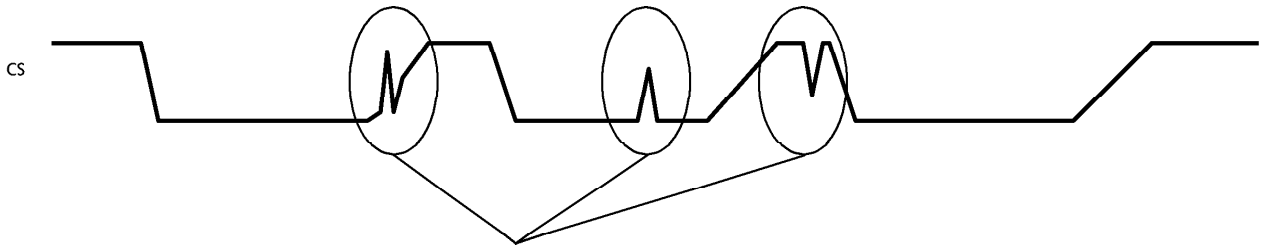
The address of the register to be accessed in consecutive Read / Write accesses is counted up in synchronization with the rising edges of CS signal. Therefore inadequate waveform and noise, as shown in the example below, could cause consecutive accesses to fail.

- Failed consecutive access due to inadequate waveform of CS



The next access starts before CS goes high and the consecutive access fails.

- Failed consecutive access due to noise on CS



The address of the register to be accessed next is erroneously counted up if CS either goes above V_{IL} during Low output or goes below V_{IH} during High output.

1.9 Monitor Pins and Their Functions

- DGATEN / SYNCO Pin (Pin 11)

This pin is used to monitor operation of internal circuits.
The signal to be monitored can be selected using DGATENSW (0Hex W01 B2).

■ DGATENSW = 0 : DGATEN monitor

Monitors internal data capture timing.

■ DGATENSW = 1 : SYNCO monitor

Monitors sync signal (C.Sync)

- ATTN Pin (Pin 10)

This pin is used either to output video attenuation signal or to monitor the system clock. The setting can be made in ATTNSW (0Hex W01 B7).

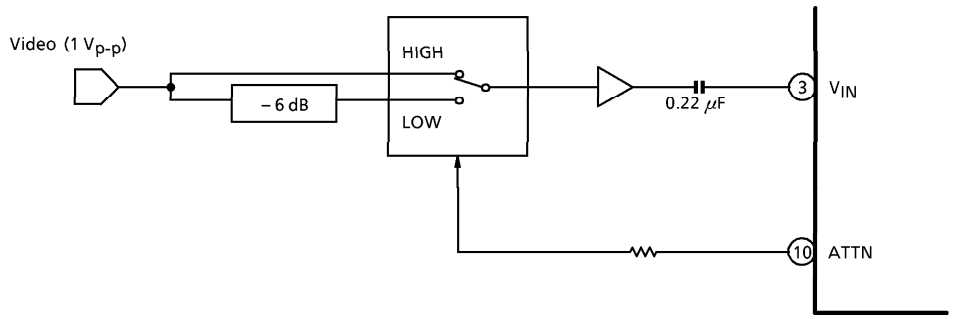
■ ATTNSW = 0 : Video attenuation signal output

The pin is used for attenuation control and thereby to prevent overflows of the transversal filter in the equalization circuit.
The pin is pulled LOW when the tap gain of the transversal filter reaches a certain value. The below chart shows an example of video attenuation control using ATTN Pin.

■ ATTNSW = 1 : System clock monitor

The pin is used to monitor the system clock (22.9 MHz) generated by an internal oscillator.

An example of control circuit using ATTN video attenuation output



2. Data Capture Function

2.1 Data Capture Mode

TC90A60U allows selection of data capture mode using control registers FC1STN (W02 B0) and FCH0G0 (W02 B1). The following explains how to use these registers.

- FC1STN (W02 B0) (initial value and recommended value : 0)

  This register is used to select whether to validate only the framing code detected first (0) or all the detected framing codes (1).
  It is recommended to usually select 0 in order to avoid erroneous detections.
  1 should be selected when detecting the position of framing codes.

- FCH0G0 (W02 B1)

  (0 : Framing Code Real-Time Regeneration Mode 1 : Consecutive Regeneration Mode)

  ■ Real-Time Regeneration Mode (initial setting)

  Usually this mode is used to detect framing codes. If a framing code is detected in the internal logic, the counter for data capture is reset. If FC1STN is set to 1, be sure to use this mode.

  ■ Consecutive Regeneration Mode

  In this mode framing code detection pulses are regenerated consecutively. The detection pulses are protected for the last 3 packets and first 2 packets. Hence, if framing code mismatch occurs in a consecutive three packets Real-Time Regeneration Mode will be automatically selected, after which if framing code mismatch does not occur for a consecutive two packets Consecutive Regeneration Mode will be selected again.

2.2 Internal Signals

- HLDA

  This signal is used to control access to RAM and can be monitored using the Read Register R00 B2. 0 indicates that the microcontroller interface is allowed to access RAM and 1 indicates that the internal circuit is allowed to.

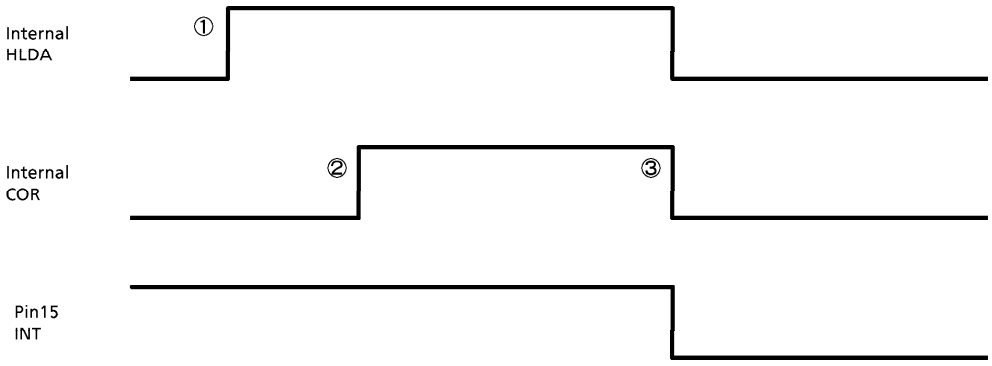
- COR

  This signal is used to select the operation status of the error correction circuit and can be monitored using the Read Register R00 B3. 0 indicates that the correction circuit is stopped and 1 indicates that it is in operation.

2.3 Internal Signal Operations

2.3.1 Automatic Error Correction Mode (default setting)

Schematic timing diagram of internal signals in Automatic Error Correction Mode



The operation status can be monitored using R00 HLDA signal monitor and COR signal monitor.

① HLDA = 0, COR = 0 : Microcontroller access is enabled.

↓

HLDA is set to 1 at the start of data capture.
At this time COR signal still remains at 0.

↓

② HLDA = 1, COR = 0 : Data capture

↓

When the data capture is complete, Capture Completion Flag in the Read Register R00 B0 is set. Then COR is set to 1 and error correction operation starts. HDLA remains at 1 during data capture.

↓

③ HLDA = 1, COR = 1 : Error correction

↓

When error correction is complete, both HLDA and COR are cleared to 0.
At this time BEST Correction Completion Flag in the Read Register R00 B1 is set and INT output is enabled.
Capture Completion Flag and BEST Correction Completion Flag will not be cleared until Operation Flag Reset in the Write Register W20 B1 is enabled.

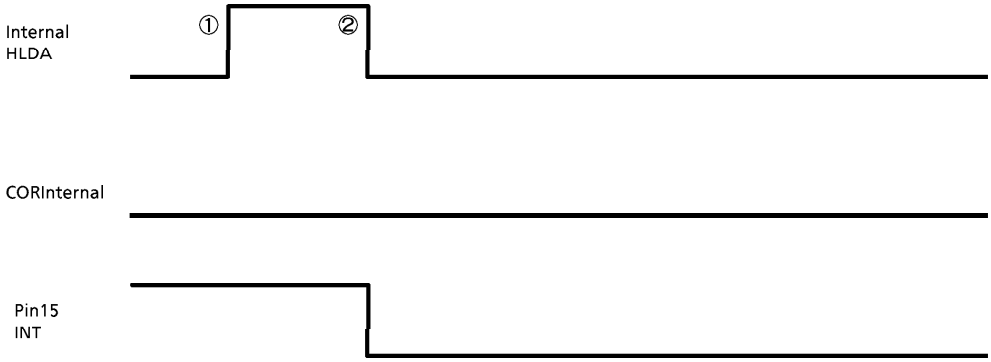
↓

The same procedure is repeated for each data capture.

2.3.2 Capture Operation Mode

The Write Register W01 B4 can be set so that error correction is not performed after data capture.

Schematic timing diagram for internal signals when error correction is not performed after data capture.



The operation status can be monitored using R00 HLDA signal monitor and COR signal monitor.

① HLDA = 0, COR = 0 : CPU access is enabled.

↓

HLDA is set to 1 at the start of data capture.

↓

② HLDA = 1, COR = 0 : Data capture

↓

When the data capture is complete, Capture Completion Flag in the Read Register R00 B0 is set. Then HDLA is cleared to 0 and INT output is enabled.

Capture Completion Flag will not be cleared until Operation Flag Reset in the Write Register W20 B1 is enabled.

↓

The same procedure is repeated for each data capture.

2.3.4 Error correction method using external control

When capture is completed in the above mode, error correction can be executed using external control.
However, this is only possible on condition that the next capture does not commence during error correction and thus requires timing management. The procedure is given below; however, Toshiba do not recommend using this method.

① Error correction can be triggered by enabling W20 HLDA and COR simultaneously on completion of capture. (W20 ← 50 Hex)

② W20 HLDA and COR must be disabled right after that (W20 ← 00 Hex).

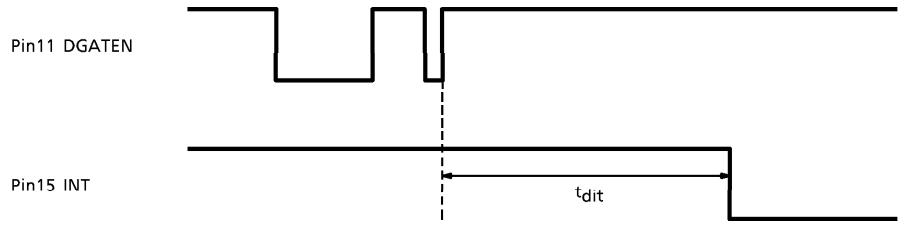
③ On completion of error correction HLDA and COR will be cleared to 0, BEST Correction Completion Flag will be set and INT output will be enabled.

2.3.5 Capture Halt Mode

By enabling W20 B5 HLDA Signal Reset the microcontroller interface is allowed to occupy the RAM. While the microcontroller is in occupation of the RAM, no capture operation is allowed. Capture operation can be re-enabled by deasserting HLDA Signal Reset. At this time it is not required to set HLDA Signal Set.

2.4 INT Signal Generation Timing

The below chart shows INT (Pin 15) signal and DGATEN (Pin 11) signal timings.



The output delay time between the last rising edge of DGATEN and the assertion of INT signal as illustrated in the above chart can be expressed as follows :

t_{dit} = Approximately 100 μs × N + 1H (approximately 63.5 μs)

Max : Approximately 870 μs

N : The number of lines to be error-corrected

(Note) : The line or lines for which Framing Code Detection Error has occurred, error correction will not be performed. For example, if Lines 10H~16H and 21H are captured and Framing Code Detection Error occurred for Lines 10H~13H, BEST correction will be performed only for Lines 14H~16H and 21H, and the output time delay can be calculated as follows :

t_{dit} = 100 × 4 + 63.5 = 463.5 μs

3. Example of Control

3.1 Example of Capture Control (using INT signal)

(Control registers are hereinafter referred to by their symbols and SW names.)

◆ STEP① System setting

Built-in sync. separation circuit	:	Used	
Automatic BEST correction	:	Performed	W01 ← 01 Hex
INT signal automatic deassertion	:	Does not deassert	
Line or lines to be captured	:	10H~16H and 21H (fixed)	W02 ← 00 Hex (Remains at initial value)

◆ STEP② Selection of the buffer or buffers to capture lines (Capture starts.)

Line Buffers 0~7 : All buffers capture.	W00 ← FFHex

◆ STEP③ Confirms capture completion after INT signal is activated.

Capture completion	R00 TFLG = "1" →OK
Error correction completion	R00 CFLG = "1" →OK
RAM available for microcontroller	R00 HLDA = "0" →OK
Error Correction Circuit not in operation	R00 COR = "0" →OK
Invalid capture	R10 = 00 Hex →OK (*1)
Invalid error correction	R11 = 00 Hex →OK (*1)

(*1) : OK if the bit corresponding to the line buffer to capture is 0.

◆ STEP③' Checks SO and CI.

Checks SI and CI for line buffers which have successfully performed error correction and selects the buffer or buffers to be read out.	Accesses R20~R2F.

◆ STEP④ Deasserts INT.

Manually deasserts INT output.	W20 INTRST ← "1" W20 INTRST ← "0"

◆ STEP⑤ Selects the line buffers to be read out and reads 1 packet consecutively.

Selects Line Buffer 0. Start address (00 Hex) is specified as byte address.	W10 ← 00 Hex W11 ← 00 Hex
24-times consecutive Read access.	Consecutively accesses R30.
Selects the next line buffer.	W10 ← 0? Hex

◆ STEP⑥ Read completion processing

Confirms that the IC did not capture data in the next field during the microcontroller's Read access.	
RAM available for microcontroller Error Correction Circuit not in operation	R00 HLDA = "0" → OK R00 COR = "0" → OK
Clears Capture Completion Flag and Error Correction Completion Flag. It is recommended that this process be carried out in STEP③ as well.	W20 FLGRST ← "1" W20 FLGRST ← "0"

3.2 Test for Read / Write Access

3.2.1 sing test registers (W70 and R70)

W70~W73 are test registers. If all the Test Pins are pulled High, writing to these registers does not affect operation. Since the values written in W70 can be read from R70, these registers can be used to check if Read / Write access is being normally performed.

3.2.2 Using Line Buffers (Test for consecutive access)

The following explains the procedure for testing consecutive Read / Write access using built-in line buffers.
Built-in line buffers are usually used for Read only ; however, it can also be written to using W30. Note that in this case the internal line buffers must be available to the microcontroller interface and cannot capture the data which is being tested.

◆ STEP① Halts capture operation.

Line buffers capture no data and the microcontroller interface occupies access.	W00 ← 00 Hex W20 ← 20 Hex

◆ STEP② Writing to Line Buffers

Selects Line Buffer 0. Start address is specified as byte address. Consecutively writes to line buffers. (e.g. 35-times consecutive Writes from 00 Hex~22 Hex in order)	W10 ← 00 Hex W11 ← 00 Hex Consecutively accesses W30.

◆ STEP③ Reading from Line Buffers

Selects Line Buffer 0. Start address is specified as byte address. Consecutively reads from line buffers. Confirms that the value read matches the value written	W10 ← 00 Hex W11 ← 00 Hex Consecutively accesses R30.

◆ STEP④ Resumes capture operation.

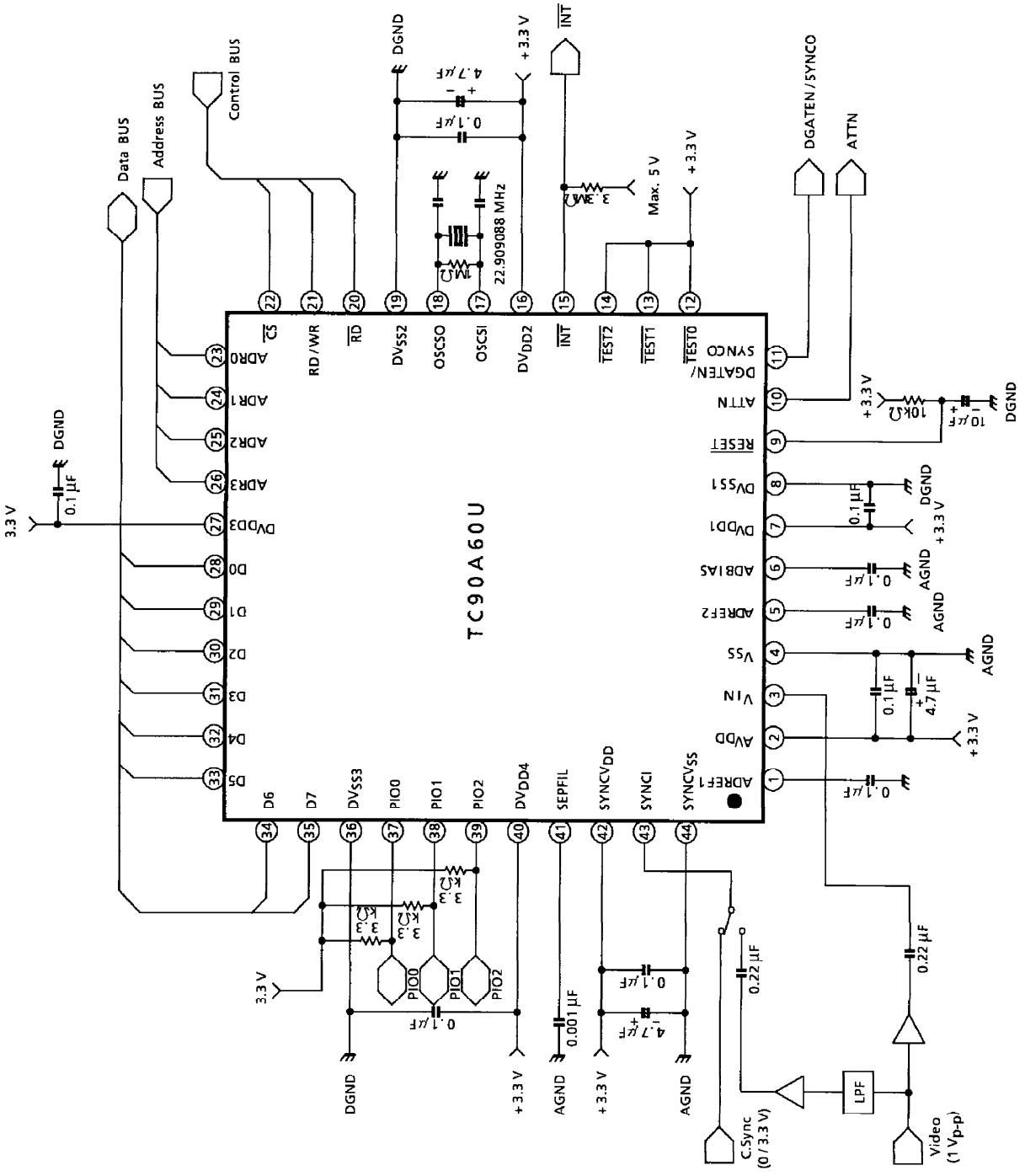
Disables occupation of access by the microcontroller interface.	W20 ← 00 Hex

MAXIMUM RATINGS (Ta = 25°C, V_{DD} = 3.3 V)

PARAMETER	SYMBOL	TEST CIR-CUIT	TEST CONDITION	APPLICABLE PINS	MIN	TYP.	MAX	UNIT
Consumption Current (for analog circuitry)	I_{DD1}	—			—	—	23	mA
Consumption Current (for digital circuitry)	I_{DD2}	—			—	—	15	mA
High-Level Input Voltage	V_{IH1}	—		(*1)	V_{DD} *0.8	—	—	V
	V_{IH2}	—		(*2)	2.4	—	5.5	V
	V_{IH3}	—		(*3)	2.4	—	—	V
Low-Level Input Voltage	V_{IL1}	—		(*1)	—	—	V_{DD} *0.2	V
	V_{IL2}	—		(*2)	—	—	0.8	V
	V_{IL3}	—		(*3)	—	—	0.8	V
High-Level Input Current	I_{IH}	—	$V_{IH} = V_{DD}$	(*1)、(*2)、(*3)	—	—	10	μA
Low-Level Input Current	I_{IL}	—	V_{IL} = GND	(*1)、(*2)、(*3)	− 10	—	—	μA
High-Level Output Voltage	V_{OH}	—	I_{OH} = − 4mA	(*4)	V_{DD} − 0.4	—	—	V
Low-Level Output Voltage	V_{OL}	—	I_{OL} = − 4mA	(*4)、(*5)	—	—	0.4	V

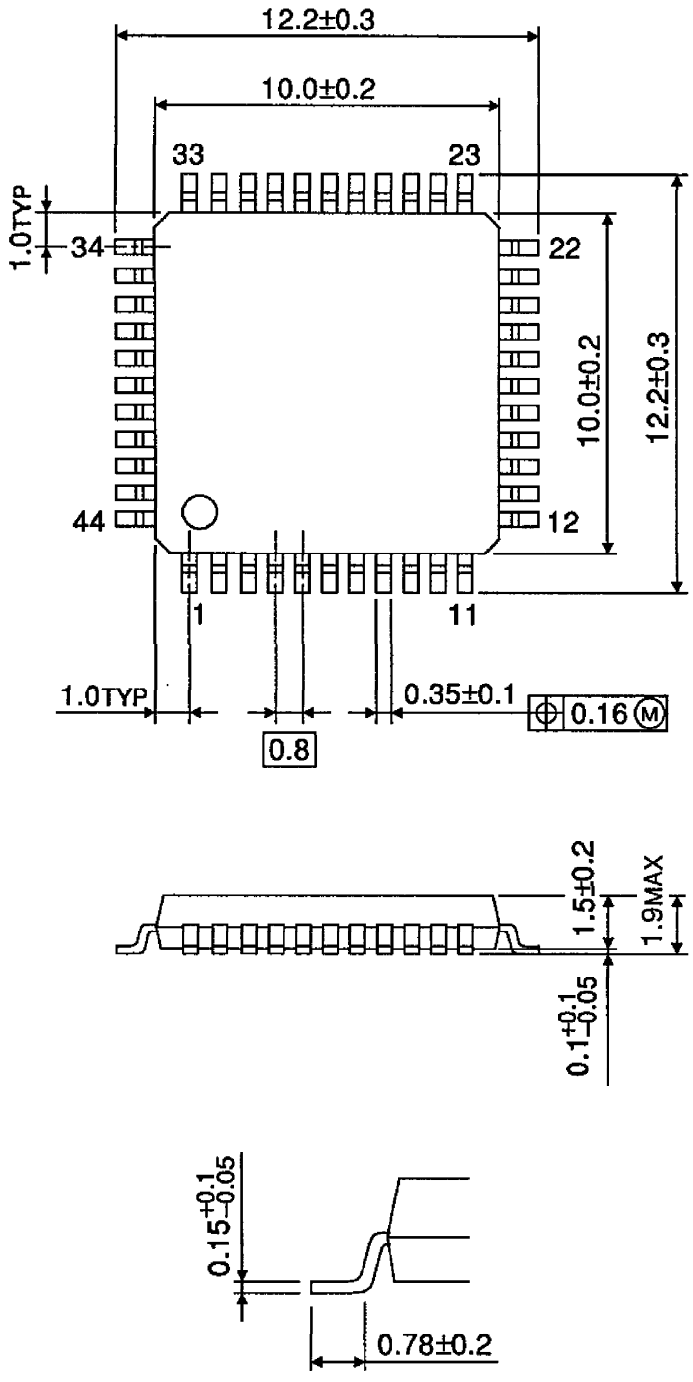
(*1) : TEST [2~0]
(*2) : ADR [3~0], D [7~0], CS, RD, RD / WR, PIO [2~ 0], RESET
(*3) : SYNCI
(*4) : D [7~0], PIO [2~0], ATTN, DGATEN / SYNCO
(*5) : INT

APPLICATION CIRCUIT EXAMPLE



PACKAGE DIMENSIONS

QFP44-P-1010-0.80 Unit : mm



Weight : 0.5 g (Typ.)